

Appl. No. 10/749,910  
Amdt. dated March 9, 2006  
Reply to Office Action of December 19, 2005

PATENT

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

1                   1.       (Currently Amended) A memory controller, comprising:  
2                   at least one bus interface, each bus interface being for connection to at least one  
3       respective device for receiving memory access requests;  
4                   a memory interface, for connection to a memory device over a memory bus;  
5                   a plurality of buffers; and  
6                   control logic, for placing received memory access requests into a queue of  
7       memory access requests,  
8                   wherein, in response to a received memory access request requiring multiple data  
9       bursts over the memory bus, data from each of said multiple data bursts is stored in a respective  
10      buffer of said plurality of buffers, and [.]  
11                  wherein, for a wrapping memory access request requiring multiple buffers, data  
12      required for a beginning and an end of the wrapping memory access request are stored in a single  
13      buffer of the plurality of buffers.

1                   2.       (Currently Amended) A memory controller as claimed in claim 1,  
2       wherein, when returning data to the respective device from which a memory access request  
3       requiring multiple data bursts over the memory bus was received, data is read out from a first  
4       part of ~~one of said buffers~~ the single buffer, then data is read out from at least one other of said  
5       buffers, then data is read out from a second part of ~~said one of said buffers~~ the single buffer.

1                   3.       (Original) A memory controller as claimed in claim 1, wherein said  
2       plurality of buffers is located in said memory interface.

1                   Claim 4. (Canceled).

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1                   5.       (Original) A memory controller as claimed in claim 1, wherein the control  
2 logic determines whether a received read access request is a wrapping request which requires  
3 multiple memory bursts, and, if so, the control logic allocates each of said memory bursts to a  
4 respective one of said buffers.

1                   6.       (Original) A memory controller as claimed in claim 1, wherein the  
2 memory controller is a SDRAM controller, and said memory interface is suitable for connection  
3 to a SDRAM memory device over said memory bus.

1                   7.       (Currently Amended) In a memory controller, comprising: at least one bus  
2 interface, each bus interface being for connection to at least one respective device for receiving  
3 memory access requests; a memory interface, for connection to a memory device over a memory  
4 bus; a plurality of buffers; and control logic, for placing received memory access requests into a  
5 queue of memory access requests, a method of retrieving data comprising:

6                   in response to a received memory access request requiring multiple data bursts  
7 over the memory bus, storing data from each of said multiple data bursts in a respective buffer of  
8 said plurality of buffers, [[.]]

9                   wherein, for a wrapping memory access request, data required for a beginning and  
10 an end of the wrapping memory access request are stored in a single buffer of the plurality of  
11 buffers.

1                   8.       (Currently Amended) A method as claimed in claim 7, further comprising  
2 when returning data to the respective device from which a memory access request requiring  
3 multiple data bursts over the memory bus was received, reading data out from a first part of one  
4 ~~of said buffers~~ single buffer, then reading data out from at least one other of said buffers, then  
5 reading data out from a second part of ~~said one of said buffers~~ the single buffer.

1                   9.       (Original) A method as claimed in claim 7, comprising storing said data  
2 from each of said multiple data bursts in a respective buffer in said memory interface.

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1                   10.     (Original) A method as claimed in claim 7, comprising storing said data  
2     from each of said multiple data bursts in a respective buffer in said bus interface to which the  
3     respective device from which the memory access request was received.

1                   11.     (Original) A method as claimed in claim 7, comprising determining  
2     whether a received read access request is a wrapping request which requires multiple memory  
3     bursts, and, if so, allocating each of said memory bursts to a respective one of said buffers.

1                   12.     (Original) A method as claimed in claim 7, wherein the memory controller  
2     is a SDRAM controller, and said memory interface receives data from a SDRAM memory  
3     device over said memory bus in SDRAM bursts.

1                   13.     (Currently Amended) A programmable logic device, wherein the  
2     programmable logic device includes a memory controller, comprising:  
3                   at least one bus interface, each bus interface being for connection to at least one  
4     respective device formed within the programmable logic device for receiving memory access  
5     requests;  
6                   a memory interface, for connection to an external memory device over a memory  
7     bus;  
8                   a plurality of buffers; and  
9                   control logic, for placing received memory access requests into a queue of  
10    memory access requests,  
11                  wherein, in response to a received memory access request requiring multiple data  
12    bursts over the memory bus, data from each of said multiple data bursts is stored in a respective  
13    buffer of said plurality of buffers, and [.]  
14                  wherein, for a wrapping memory access request, data required for a beginning and  
15    an end of the wrapping memory access request are stored in a single buffer of the plurality of  
16    buffers.

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1                   14.   (New) A memory controller as recited in claim 1, wherein each of the  
2 plurality of buffers includes a plurality of sub-buffers, data required for the beginning and the  
3 end of the wrapping memory access request being stored in separate sub-buffers of the single  
4 buffer.

1                   15.   (New) A memory controller as recited in claim 14, wherein the control  
2 logic is operable to record the value of a pointer indicating the sub-buffer from which data  
3 required for the end of the wrapping memory is to be retrieved from the single buffer.

1                   16.   (New) A method as recited in claim 7, wherein each of the plurality of  
2 buffers includes a plurality of sub-buffers, data required for the beginning and the end of the  
3 wrapping memory access request being stored in separate sub-buffers of the single buffer.

1                   17.   (New) A method as recited in claim 16, wherein the control logic is  
2 operable to record the value of a pointer indicating the sub-buffer from which data required for  
3 the end of the wrapping memory is to be retrieved from the single buffer.